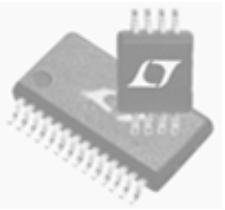
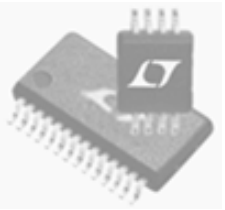


# PoE Plus
# IEEE 802.3at
# Classification Ad Hoc
# Extended Classification Using Two Classification Events

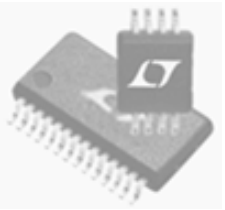
Clay Stanford
Linear Technology
Sept 11, 2007
Seoul

# Problem Discovered in Protocol



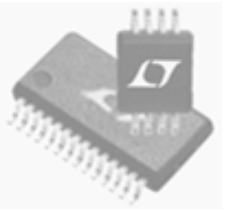
- The proposed 2-Event Classification protocol has a problem:
  - Using a compliant Type 1 (802.3af) PSE
  - Using a compliant Type 2 (802.3at) PD
  - When a Type 2 PD is plugged into a Type 1 PSE, possible for PD to incorrectly interpret waveform as the 2-Event Classification mechanism

# Solution



- Do Not Allow 25K During Mark
  - PSE would fail detection during Mark period
  - PSE would return to Idle State (Vport<2.8V)
  - PD State engine would be reset
  - No false Identification

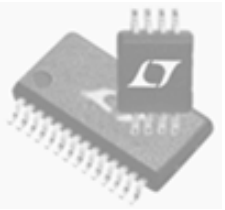
# Revised Presentation of 2-Event Classification Mechanism



- The following slides are provided for reference and are identical to San Francisco except

- Page 13: 2nd Mark Max Removed.
- Page 14: Note was added explaining Class Event 3 behavior.
- Page 15: PD Behavior During Mark, added Table 33-9.
- Page 18: State digram added for Type 2 Physical Layer PSE
- Page 19: State diagram added for Type 2 LLDP PSE

# Motion to Implement Change

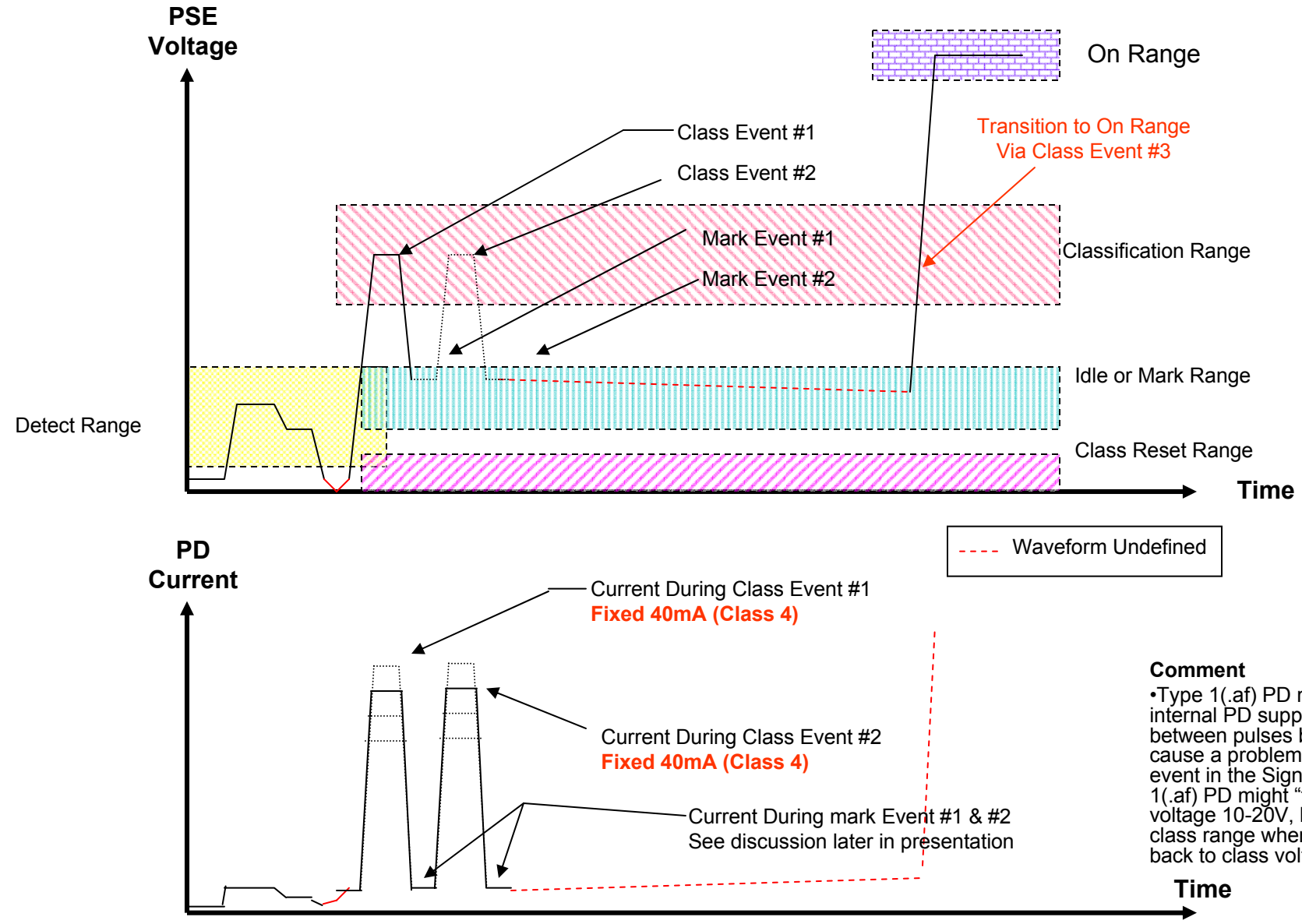


Motion by Clay Stanford
Seconded by XXXX

The 802.3at Task Force accepts page 13, 14, 15, 18, and 19 of presentation stanford1.pdf presented Sept 11, 2007 and instructs the editor to implement this change in the draft.

| All in room: | 802.3 Voters Only: |
|---|---|
| For: XX | For: XX |
| Against: XX | Against: XX |
| Abstain: XX | Abstain: XX |

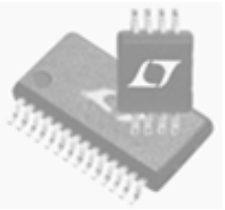
# 802.3at Classification Using Two Classification Events




**Comment**

•Type 1(.af) PD may not pull internal PD supply down quickly between pulses but this doesn't cause a problem. With the Mark event in the Signature range, Type 1(.af) PD might "float" at some voltage 10-20V, but will return to class range when PSE drives port back to class voltage.

# PoEP: IEEE 802.3at
# Two Event Rules



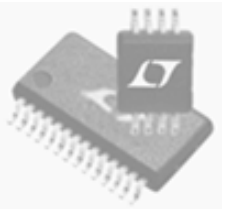
## Type 2 (.at) PD Rules:

- PD is behind diode bridge so fall time is controlled by internal PD circuits and not PSE port voltage. Therefore a Type 2 (.at) PD is required to pull the internal supply down using the classification event current until the PD detects the Mark event. Once the PD has detected the Mark, the PD can stop pulling down on the port. Note that in this scenario, the port voltage may not discharge all the way down to the Mark range and this is not a problem.
- If the port voltage goes to reset range, PD state engine is reset and the PD will go to the detect state.

## Type 2 (.at) System Rules:

- Type 2 (.at) PSE is the master, generating port voltage. Type 2 (.at) PD is slaved to Type 2 (.at) PSE , responding with port current.
- System is designed so that Type 2 (.at) PD spends a limited amount of time in the Mark range in case Type 2 (.at) PD is using dynamic memory which requires power to maintain state.
- Type 2 (.at) PSE must transition from 2$^{nd}$ event through Class Event 3 to Power On without going down into Reset range.

# PoEP: IEEE 802.3at
# Two-Event Type 1/2 (.af/.at) Interaction



**Type 2 (.at) PSE with Type 1 (.af) PD:**

- If a Type 2(.at) PSE sees class 0, 1, 2, or 3, it assumes Type 1(.af) PD and powers per .af spec, i.e. 15.4W, 4W, 7W, 15.4W respectively.
  - Note: Type 1(.af) PD that uses class 4 (in error) will get powered with 30W by a Type 2(.at) PSE. This is a minor annoyance with this class scheme and is considered acceptable.
  - If a Type 2(.at) PSE sees class 4, and it is using layer 1 only for classification, it must ping twice.
  - If a Type 2(.at) PSE sees class 0,1,2, or 3, it has the option of pinging either one or two times.

May06 motion to include 2W class and July06 motion for ~9W class will not be supported.

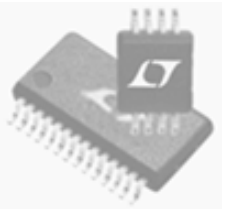
**Type 2(.at) PSE with Type 2(.at) PD:**

- Type 2(.at) PSEs should see class 4 when connected to a Type 2(.at) PD.
- Type2(.at) PSE only using L1 will ping twice to signal to the Type 2(.at) PD that it is a Type 2 PSE.
- If a Type 2(.at) PSE sees inconsistent class results (i.e. 4-1, 4-2, etc), the behavior is non-compliant and PSE action is undefined.

**.Type 1 (.af) PSE with Type 2 (.at) PD:**

- If a Type 1(.af) PSE sees a Type 2 (.at) PD, it will see class 4 and power at 15.4W.

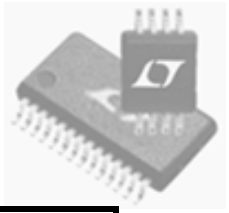
# Motion from March 2006



The IEEE 802.3at Task Force affirms that a PD requiring more than 12.95W will support a Layer-1 Classification extension and a Layer-2 Classification mechanism.

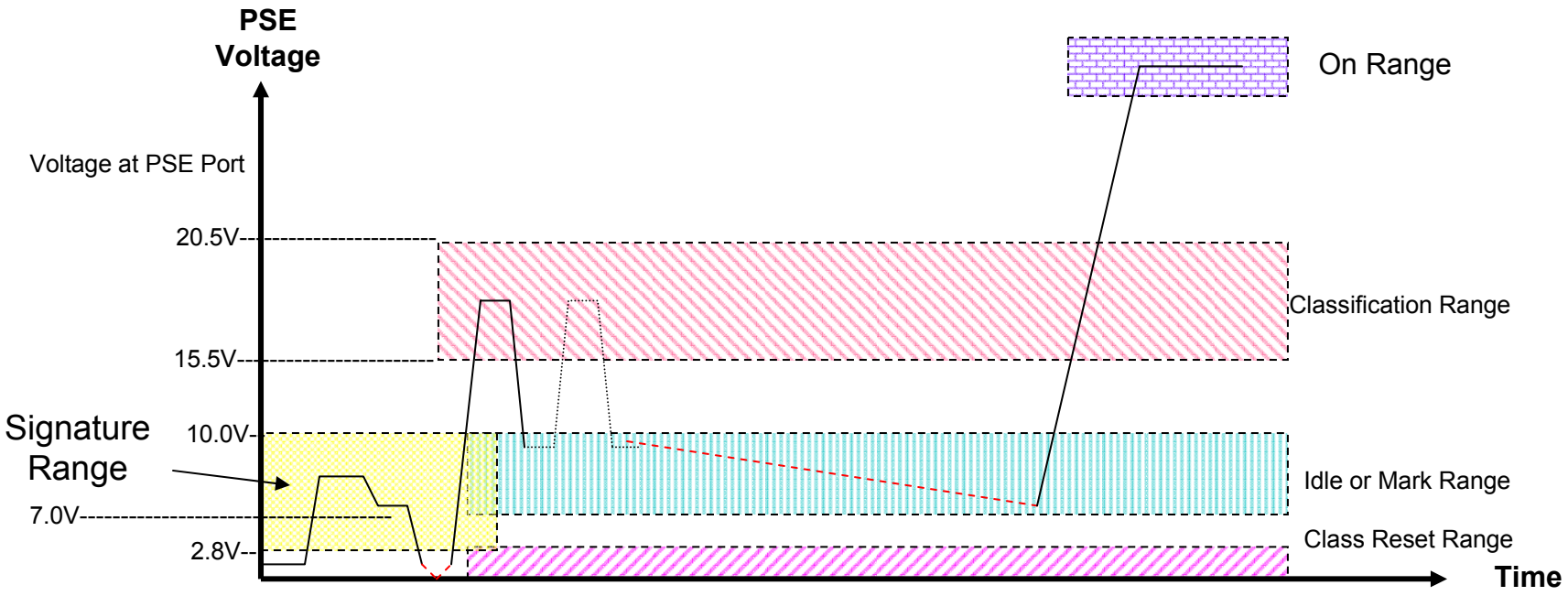
Endpoint PSEs must support Layer-2 classification or Layer-1 classification extension for PDs requiring more than 12.95W.

# All Possible PSE/PD Combinations

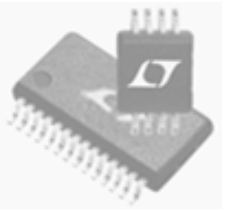


| PSE TYPE | PD TYPE | COMMENTS |
|---|---|---|
| Type 1(.af) | Type 1(.af) | Existing 802.3af system, class 0, 1, 2, or 3. |
| Type 1(.af) | Type 2(.at) | Type 1(.af)PSE sees class 4 and powers per 802.3af specification, i.e. 15.4W. Type 2(.at) PD can only assume Type 1 PSE and must operate with 15.4W and alert user not enough power. |
| Type 2(.at) L1<br>i.e. high power midspan | Type 1(.af) | Type 2(.at) PSE sees class 0, 1, 2, 3 and powers per 802.3af specification. |
| Type 2(.at) L1<br>i.e. high power midspan | Type 2(.at) | Type 2(.at) PSE sees class 4 and powers with maximum allowable 802.3at power level. Type 2(.at) PD sees two class pings and knows Type 2 PSE connected. Power information is known before PD is powered. |
| Type 2(.at) L2<br>i.e. end point PSE | Type 1(.af) | Type 2(.at) PSE sees class 0, 1, 2, 3 and powers per 802.3af specification. Layer 2 communication fails to establish. Power level is maintained at .af levels. PD sees af behavior and operates under .af specs. |
| Type 2(.at) L2<br>i.e. end point PSE | Type 2(.at) | Type 2(.at) PSE sees class 4 and powers with 15.4W. Layer 2 communication is established and mutual identification is established. High power operation begins. |

# Voltage Ranges and Timing Specification



# PSE and PD Voltage Ranges



| PSE VOLTAGE SPECIFICATIONS | | |
|---|---|---|
| FUNCTION | MIN (V) | MAX(V) |
| Classification | 15.5[1] | 20.5[1] |
| Mark | 7.0 | 10 |
| Low Reset Range | 0 | 2.8[1] |
| High Reset Range | -- | -- |

| PD VOLTAGE SPECIFICATIONS | | |
|---|---|---|
| FUNCTION | MIN (V) | MAX(V) |
| Classification | 14.5[1] | 20.5[1] |
| Mark | 6.9[2] | 10[3] |
| Low Reset Range | 0 | 2.8[3] |
| High Reset Range | 30[1,4] | |

## Notes on Calculations

1. Value from 802.3af specification.
2. Assume cable max resistance = 20ohms so as to also work with .af systems.
   Cable drop max = 2mA (mark current max) * 20ohms = .04V~=0.1V.
   With 7V at PSE, may only be ~6.9V at PD.
3. PD Mark and Reset limits are not equivalent to PD signature range (2.7V-10.1V). PD upper limits are equal to PSE upper limits.
4. Reset high occurs when powered PD drops below PD power supply turn off voltage.

# Timing Specification

| TIMING SPECIFICATIONS | | |
|---|---|---|
| EVENT | MIN (ms) | MAX (ms) |
| 1st Class | 6 | 30 |
| 1st Mark | 6 | 12 |
| 2nd Class | 6 | 30 |
| 2nd Mark | 6 | Blank* |
| TOTAL (for reference only) | 24ms | 84ms |

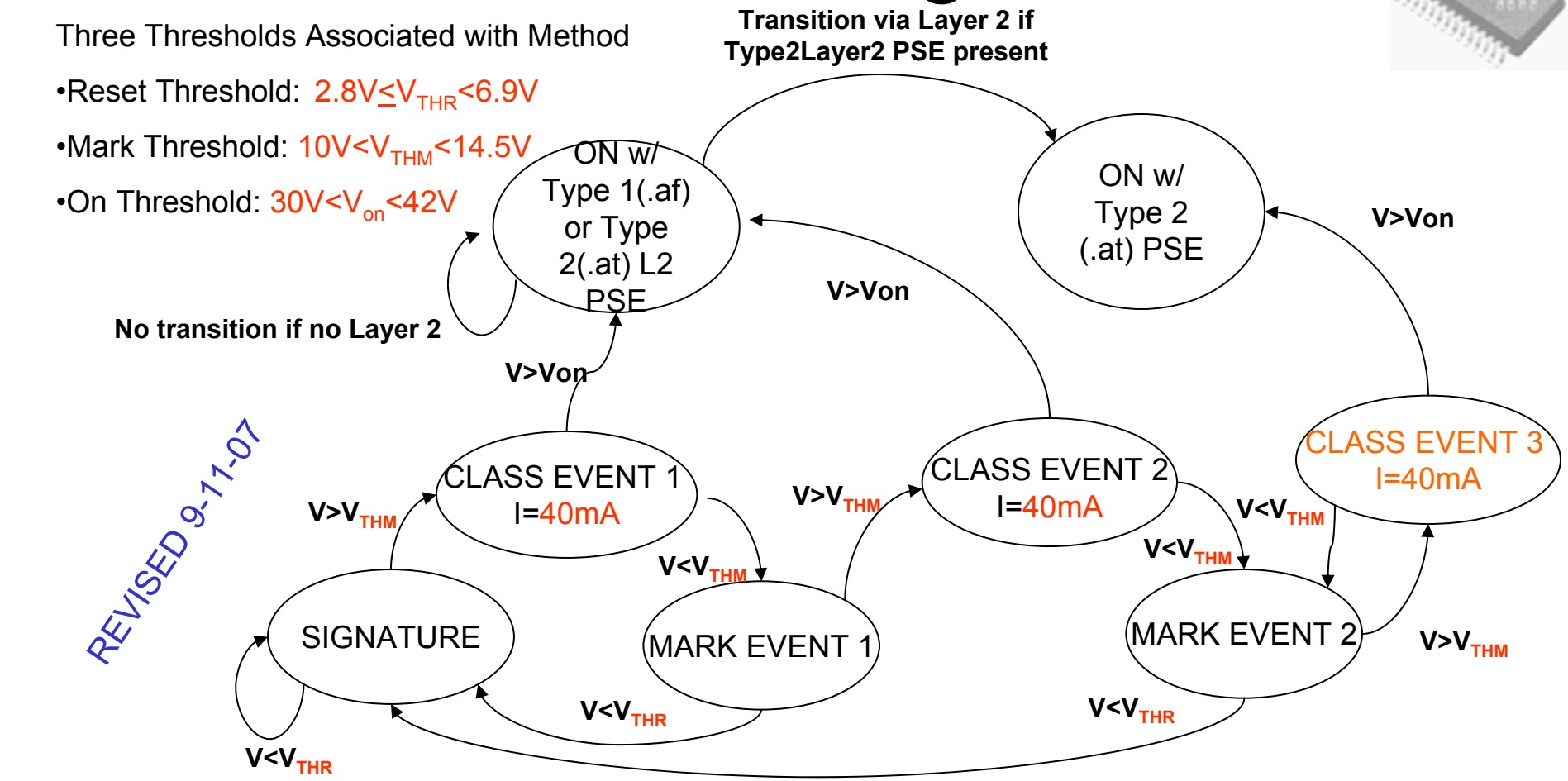
*Note 1. Time from end of detection until power on is limited by section 33.2.8.13. This in turn limits 2nd Mark.

REVISED 9-11-07

# Classification State Engine in PD

Three Thresholds Associated with Method

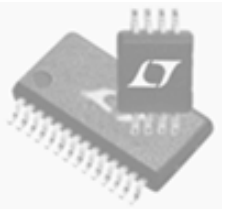
- Reset Threshold: $2.8V \leq V_{THR} < 6.9V$
- Mark Threshold: $10V < V_{THM} < 14.5V$
- On Threshold: $30V < V_{on} < 42V$




Class Event 3 creates a defined behavior for a Type 2 PD which is brought into the classification range repeatedly.

In a typical power-on event, the PI voltage will transition from Mark Event range directly through Classification range to Power On. Class Event 3 durations less than Tclass may not allow a Type 2 PD to respond with a Classification current. There is no minimum Class Event 3 time duration and for Class Event 3 times less than Tclass, there is no requirement for a Type 2 PD to respond with a defined current.

# PD Behavior During Mark Event



PD current: $0.25mA < I_{PD} < 2.0\ mA$

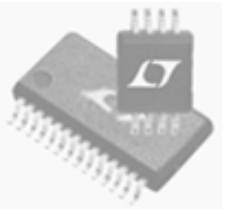
**AND** PD 2-point signature non-valid per Table 33-9

Table 33–9—Non-valid PD detection signature characteristics, measured at PD input connector

| Parameter | Conditions | Range of values | Unit |
|---|---|---|---|
| V-I Slope | V < 10.1V | Either greater than 45 or less than 12 | KΩ |
| Input Capacitance | V < 10.1V | Greater than 10 | μF |

REVISED 9-11-07

# PD Current



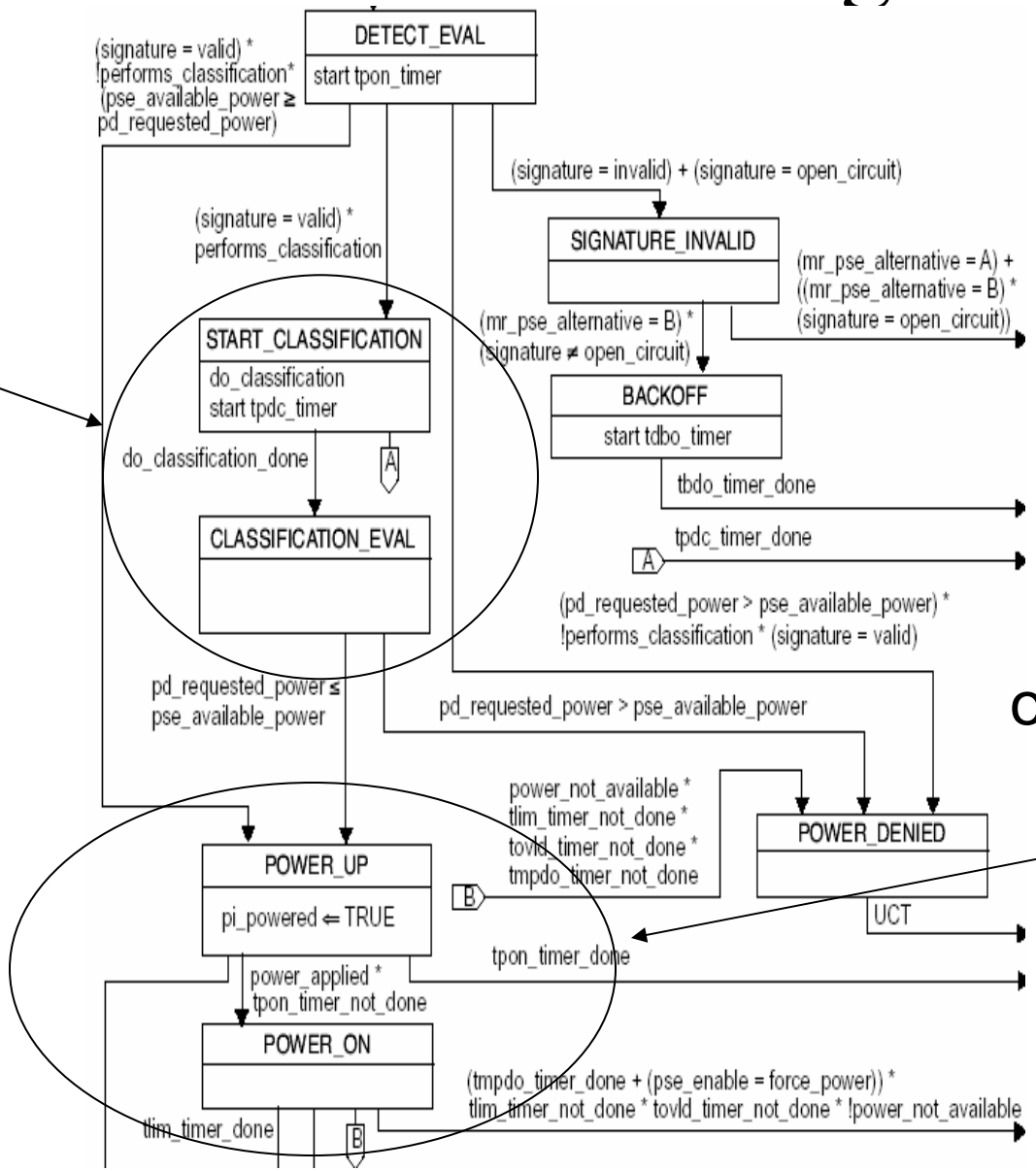
With Type 2 PDs, the current is a function of the state of the PD*:

- Type 2 PDs will draw Class 4 current when in the Class state. The port voltage while in the Class state can range from 20.5V down to near 10V, depending on implementation.
- Type 2 PDs will draw 0.25-2mA when in the Mark state. The port voltage while in the Mark state can range from 7V up to near 15.5V, depending on implementation.

*The state of the PD transitions based on port voltage.

# Existing 802.3af PSE State Engine

Expansion of Classification Function




Expansion of Power On Function

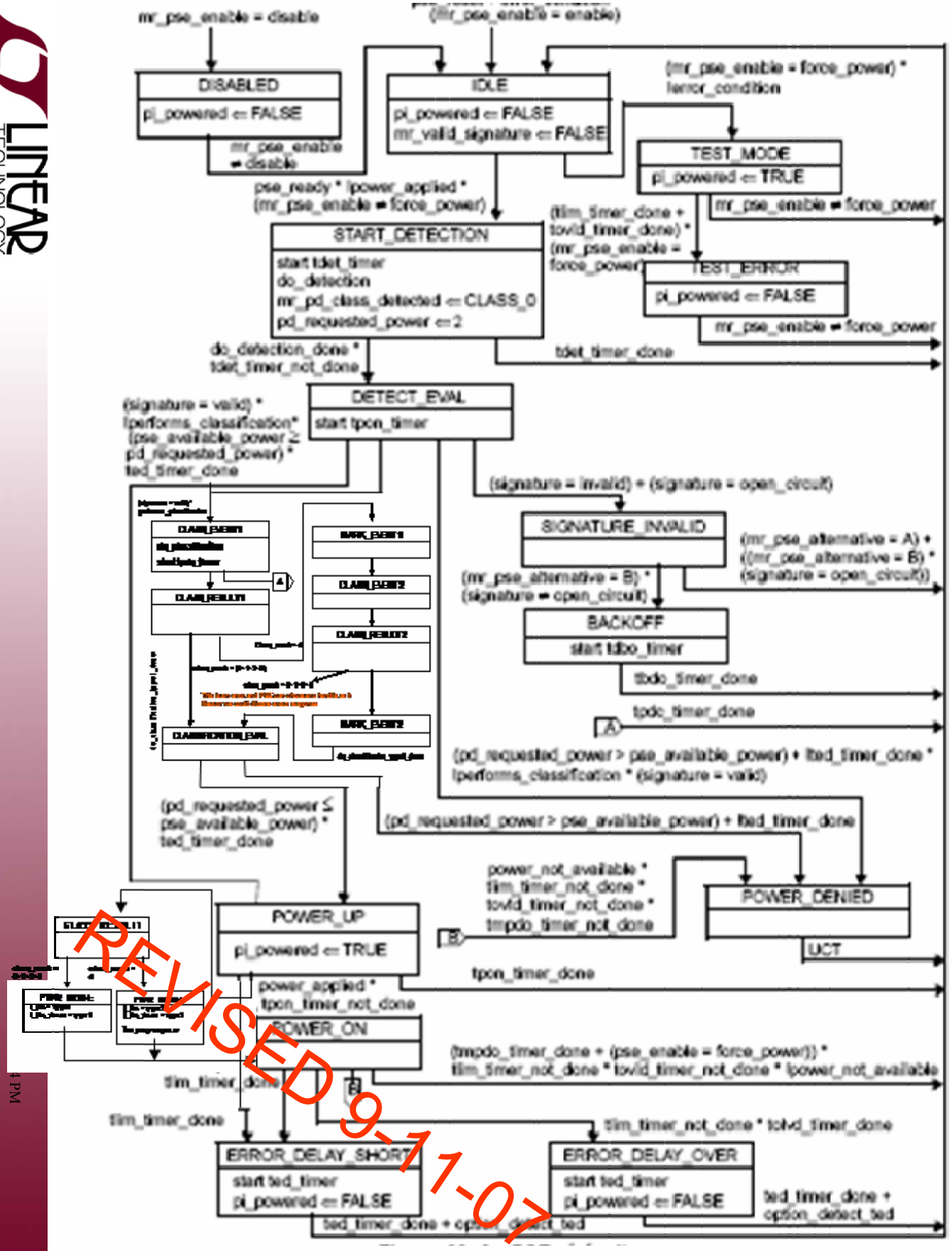



Figure 33-6b Type 2 Physical Layer PSE state diagram

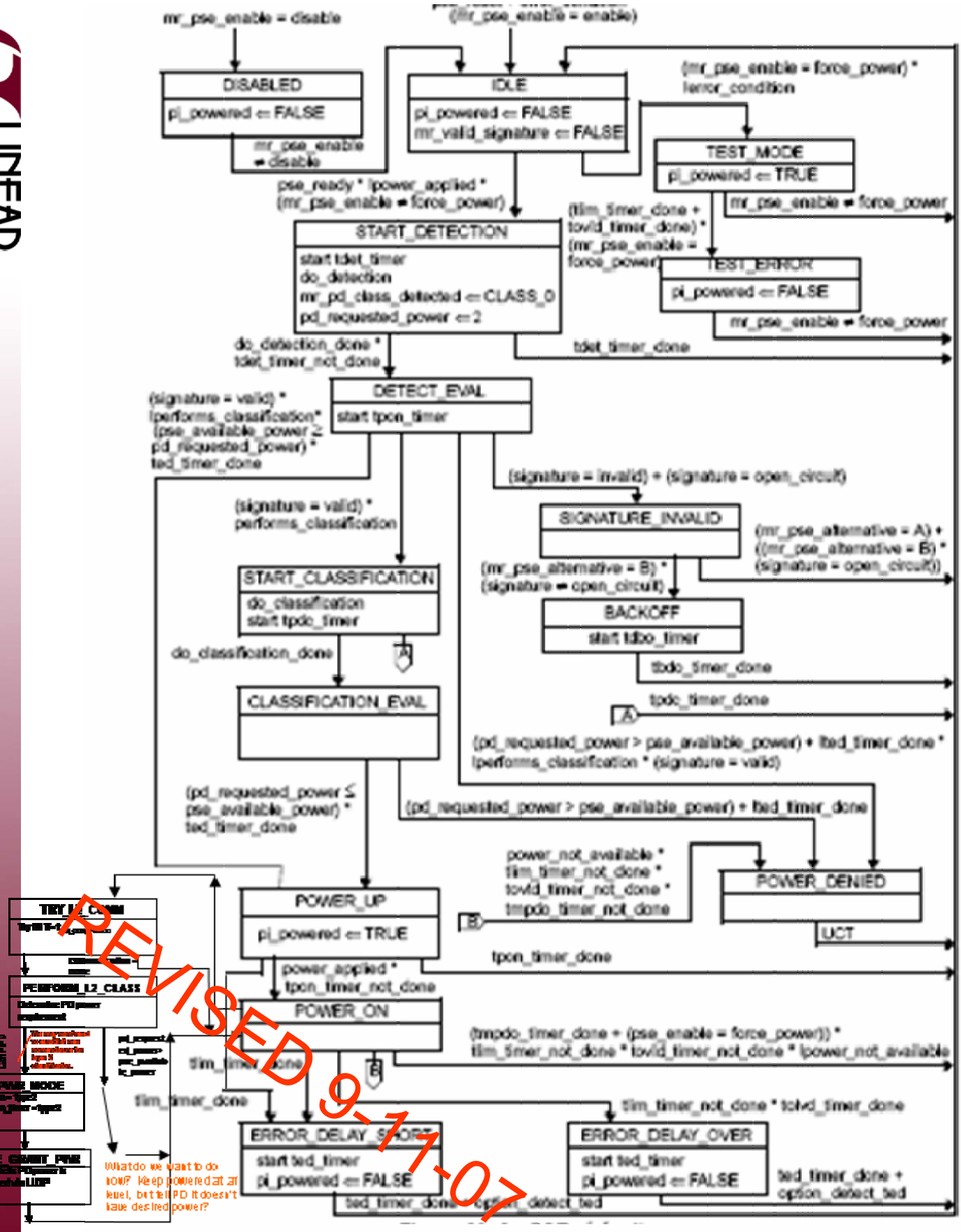
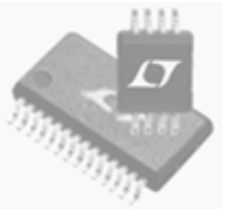
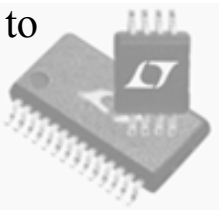



Figure 33-6c Type 2 LLDP PSE state diagram

# Addendum



Supporting Material



dt max = (C/I) dv
= (.66uF / 36mA) (20.5-10)
= 0.19ms max i.e. OK

Discharge of port from Class state to Mark state must occur within the Mark minimum time (6ms).

When the PD detects the Mark event, PD changes to Mark state. PD current is reduced and further port discharge is at a slower rate. The port is not required and may not discharge into the Mark range. Any of the depicted waveforms may occur and are acceptable.

$V_{PSE}$

20.5V max→

Class Range

15.5V min→

10.0 max→

Mark Range

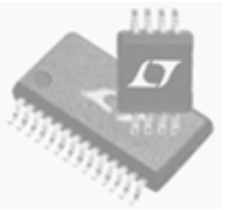
7.0V min→

Class Event 1
I= 36-44mA

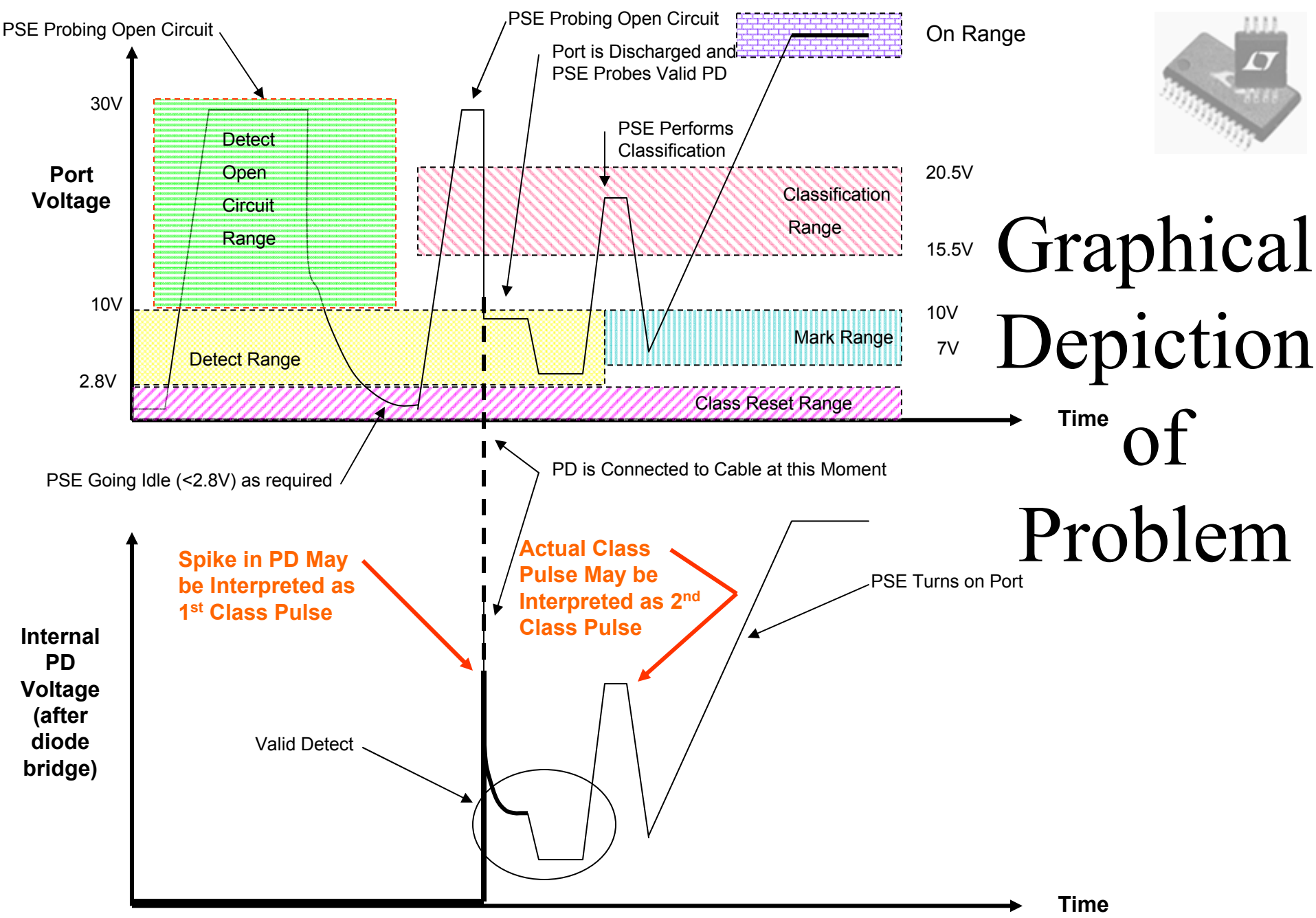
Mark Event 1
I= 0.25-2mA

# Worst-Case Discharge Timing Calculations Waveform Clarification PD Current Clarification

# Details of Problem

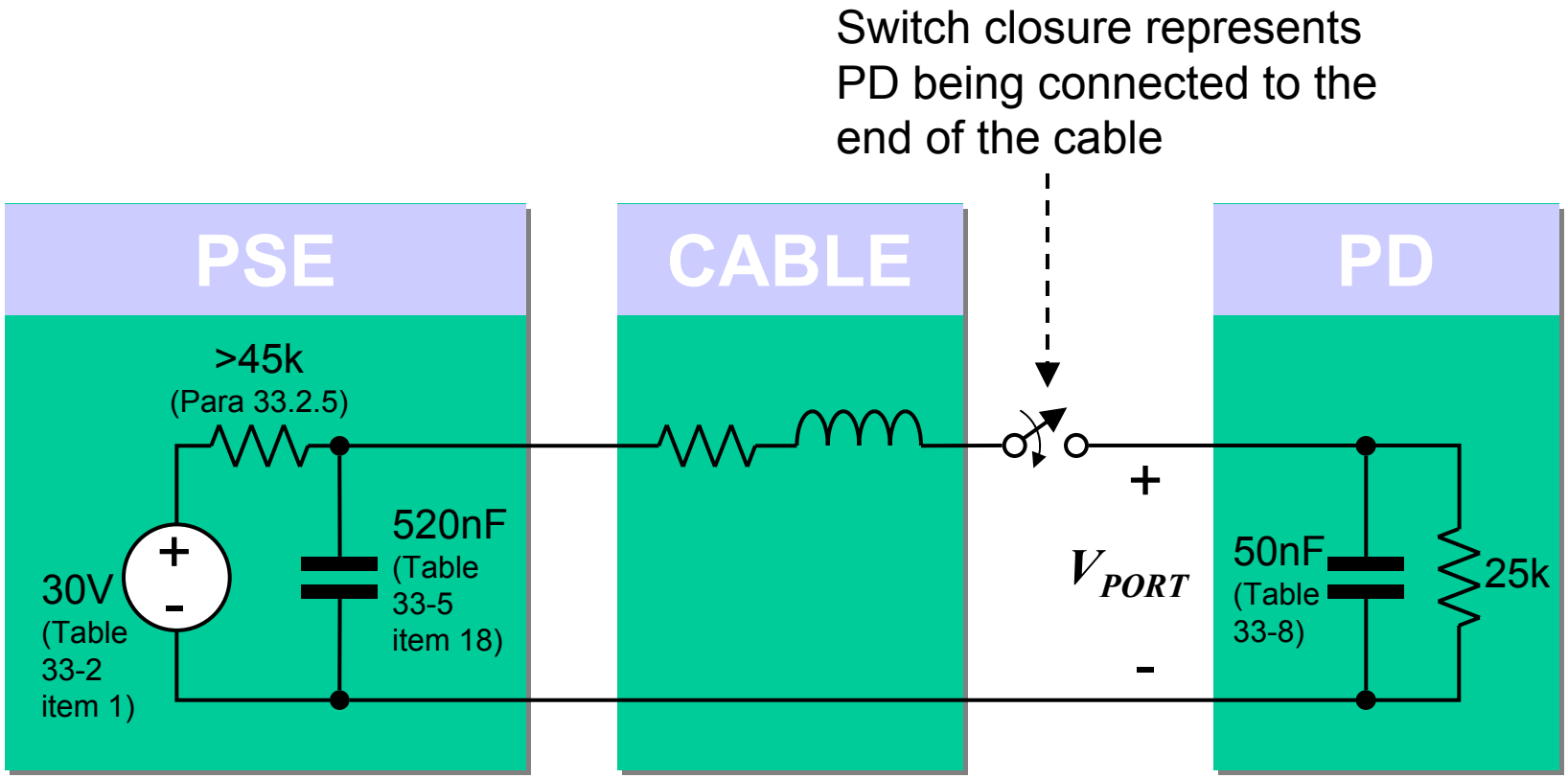


- When a PSE is probing an open circuit, port voltage can go to 30V (Table 33-2, item 1)
- At the moment the Type 2 PD is connected to the cable, internal PD voltage can exhibit a spike similar to a classification pulse (refer to sample waveform)
- This spike can fool the PD state machine into thinking the first classification event has occurred
- After detection, Type 1 PSE may perform classification which would appear to Type 2 PD as the second classification event.
- Type 2 PD would incorrectly conclude that Type 2-Layer 1 PSE is present

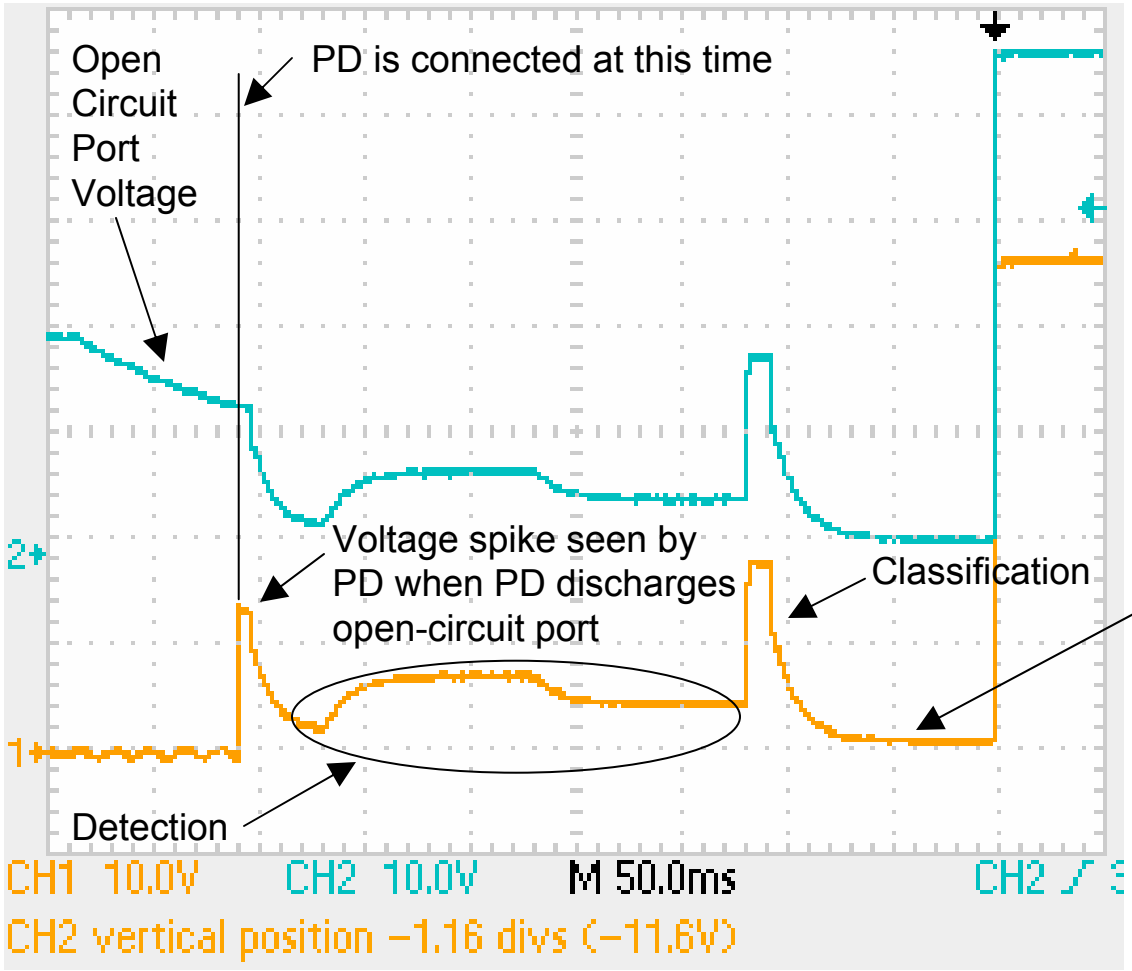



# Graphical Depiction of Problem

# Worst-Case Open-Circuit Port Model



# Experimental Waveform




$V_{PORT}$

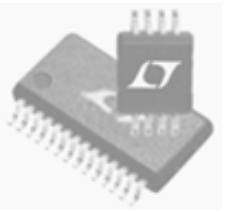
$V_{PD\_INTERNAL}$

In this example, port goes to 0V which would reset the PD state machine. However, that is not required per IEEE 802.3af

# PD/PSE State Machines

Three Thresholds Associated with Method

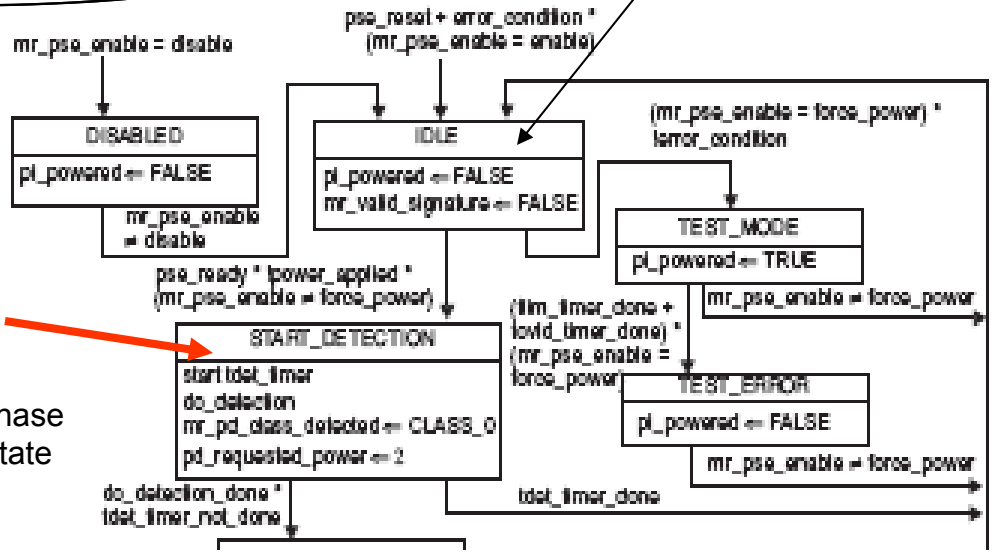
- Reset Threshold: $2.8V \leq V_{THR} < 6.9V$
- Mark Threshold: $10V < V_{THM} < 14.5V$
- On Threshold: $30V < V_{on} < 42V$






PD State Machine Depends on PSE going to Idle State

PSE Idle State is defined as Vport<2.8V




When plugging in PD, possible to Enter PSE State Diagram Here

If PD Plugged in after Idle State and Before Detection Phase 1 is complete, PD can see spike and may not see Idle State (used for PD Reset).